Silicon Diffused Power Transistor BUJ100AT

GENERAL DESCRIPTION

High-voltage, high-speed planar-passivated npn power switching transistor in the SOT223 envelope intended for use in compact fluorescent lamps, low power electronic lighting ballasts and similar high frequency converters and inverters.

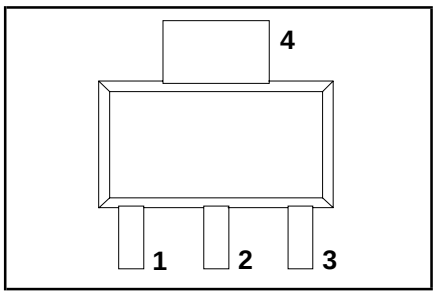
QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	TYP.	MAX.	UNIT
V_{CESM}	Collector-emitter voltage peak value	V_{BE} = 0 V	-	700	V
V_{CBO}	Collector-Base voltage (open emitter)		-	700	V
V_{CEO}	Collector-emitter voltage (open base)		-	400	V
I_C	Collector current (DC)		-	1.0	A
I_{CM}	Collector current peak value		-	2.0	A
P_{tot}	Total power dissipation	$T_{sp} \leq 25$ ˚C	-	6	W
V_{CEsat}	Collector-emitter saturation voltage	I_C = 0.75 A;I_B = 150 mA	0.23	1.0	V
h_{FE}		I_C = 0.75 A;V_{CE} = 5 V	14	20	
t_{fi}	Fall time (Inductive)	I_C = 1.0 A,I_{BON}=200 mA	50	70	ns

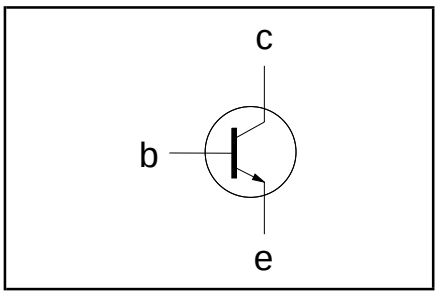
PINNING - SOT223

PIN	DESCRIPTION
1	base
2	collector
3	emitter
4	collector (tab)

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum Rating System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CESM}	Collector to emitter voltage	V_{BE} = 0 V	-	700	V
V_{CEO}	Collector to emitter voltage (open base)		-	400	V
V_{CBO}	Collector to base voltage (open emitter)		-	700	V
I_C	Collector current (DC)		-	1.0	A
I_{CM}	Collector current peak value		-	2.0	A
I_B	Base current (DC)		-	0.5	A
I_{BM}	Base current peak value		-	1.0	A
P_{tot}	Total power dissipation	$T_{sp} \leq 25$ ˚C	-	6	W
T_{stg}	Storage temperature		-65	150	˚C
T_j	Junction temperature		-	150	˚C

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	TYP.	MAX.	UNIT
$R_{th\ j\text{-}sp}$	Junction to solder point		-	20	K/W
$R_{th\ j\text{-}a}$	Junction to ambient	pcb mounted pad areas as in Fig. 23)			
		pcb mounted, minimum footprint	70	-	K/W
		Mounted on 50x34x2mm aluminium PCB	30	-	K/W

STATIC CHARACTERISTICS

T_{sp} = 25 ˚C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{CES},I_{CBO}	Collector cut-off current [1]	V_{BE} = 0 V; V_{CE} = $V_{CESMmax}$	-	2.5	100	µA
I_{CES}		V_{BE} = 0 V; V_{CE} = $V_{CESMmax}$; T_j = 125 ˚C	-	15	500	µA
I_{CEO}	Collector cut-off current	V_{CE} = $V_{CESMmax}$(400V)	-	-	100	µA
I_{EBO}	Emitter cut-off current	V_{EB} = 9 V; I_C = 0 A	-	0.02	100	µA
$V_{CEOsust}$	Collector-emitter sustaining voltage	I_B = 0 A; I_C = 10 mA; L = 25 mH	400	-	-	V
V_{CEsat}	Collector-emitter saturation voltage	I_C = 0.75 A; I_B = 0.15mA	-	0.23	1.0	V
V_{BEsat}	Base-emitter saturation voltage	I_C = 0.75 A; I_B = 0.15mA	-	0.95	1.3	V
h_{FE}	DC current gain	I_C = 10mA; V_{CE} = 5 V	11	20	27	
h_{FE}		I_C = 100mA; V_{CE} = 5 V	12.5	21	31	
h_{FE}		I_C = 0.75A; V_{CE} = 5 V	9	14	20	

DYNAMIC CHARACTERISTICS

T_{sp} = 25 ˚C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	TYP.	MAX.	UNIT
	Switching times (resistive load)	I_{Con} = 1.0 A; I_{Bon} = -I_{Boff} = 200mA; R_L = 75 ohms; V_{BB2} = 4 V;			
t_{on}	Turn-on time		0.65	0.88	µs
t_s	Turn-off storage time		0.88	1.2	µs
t_f	Turn-off fall time		250	338	ns
	Switching times (inductive load)	I_{Con} = 1.0 A; I_{Bon} = 200mA; L_B = 1 µH; -V_{BB} = 5 V			
t_s	Turn-off storage time		0.51	0.7	µs
t_f	Turn-off fall time		50	70	ns
	Switching times (inductive load)	I_{Con} = 1.0 A; I_{Bon} = 200mA; L_B = 1 µH; -V_{BB} = 5 V; T_j = 100 ˚C			
t_s	Turn-off storage time		-	1.4	µs
t_f	Turn-off fall time		-	130	ns

1 Measured with half sine-wave voltage (curve tracer).

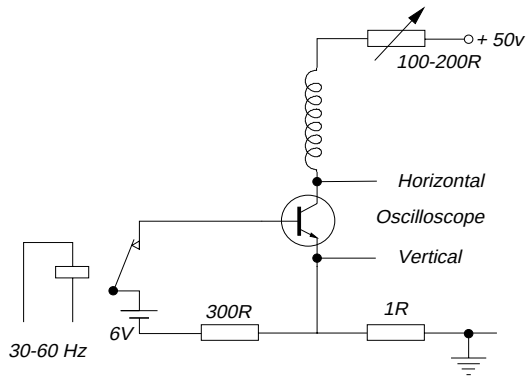


Fig.1. Test circuit for $V_{CEOsust}$.

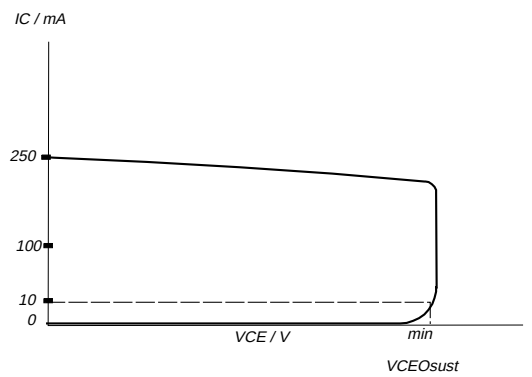


Fig.2. Oscilloscope display for $V_{CEOsust}$.

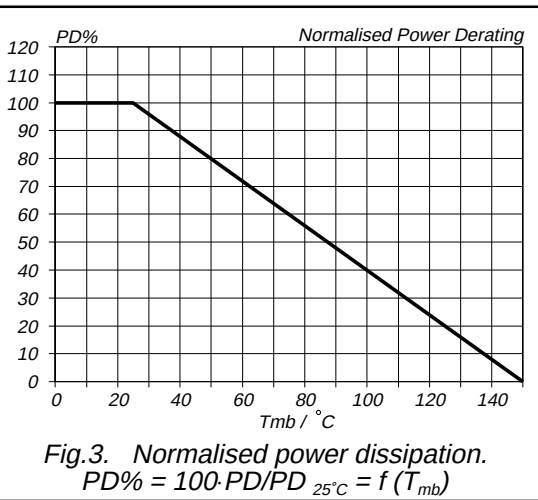


Fig.3. Normalised power dissipation. PD% = 100·PD/PD $_{25°C}$ = f (T_{mb})

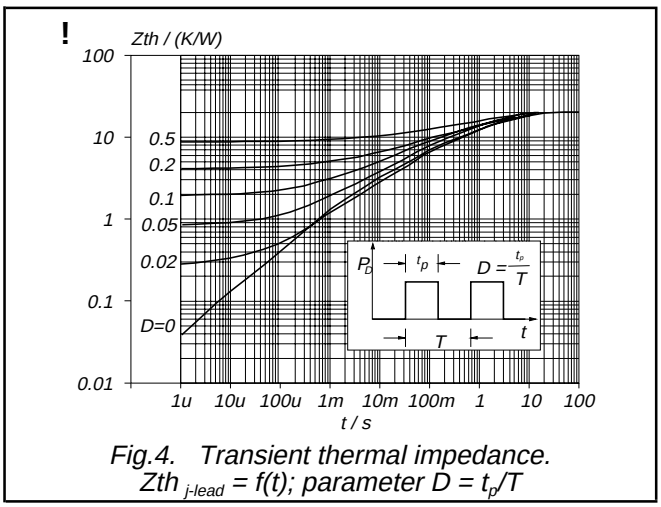


Fig.4. Transient thermal impedance. Zth $_{j\text{-}lead}$ = f(t); parameter D = t_p/T

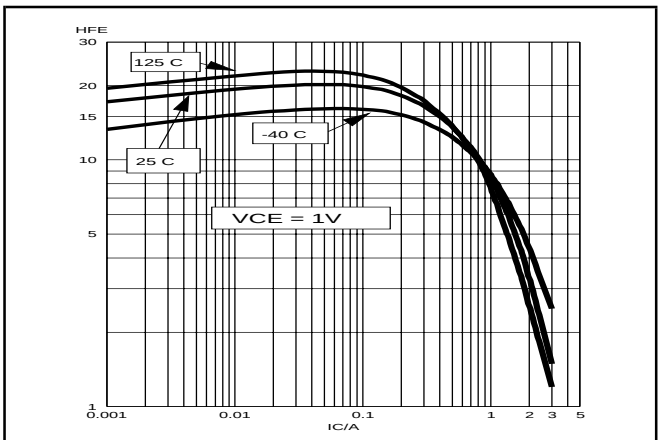


Fig.5. Typical DC current gain. h_{FE} = f(I_C) parameter V_{CE}

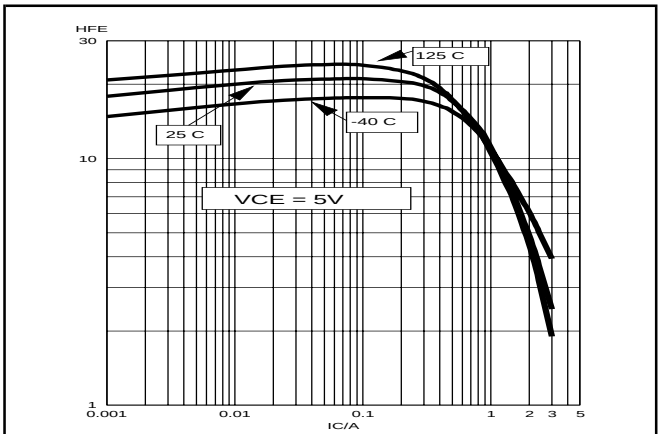


Fig.6. Typical DC current gain. h_{FE} = f(I_C) parameter V_{CE}

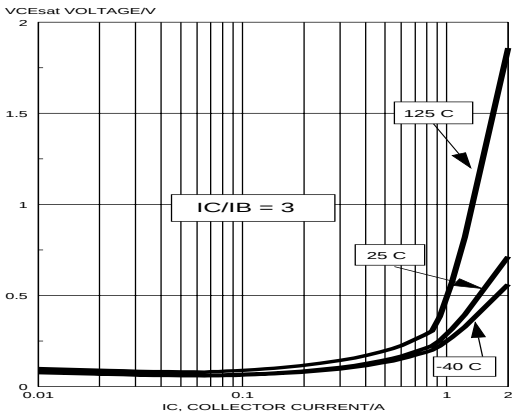


Fig.7. Collector-Emitter saturation voltage. Solid Lines = typ values, $I_C/I_B = 3$

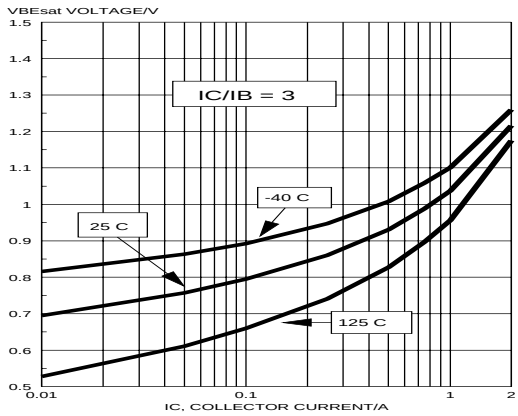


Fig.8. Base-Emitter saturation voltage. Solid Lines = typ values, $I_C/I_B = 3$

INDUCTIVE SWITCHING

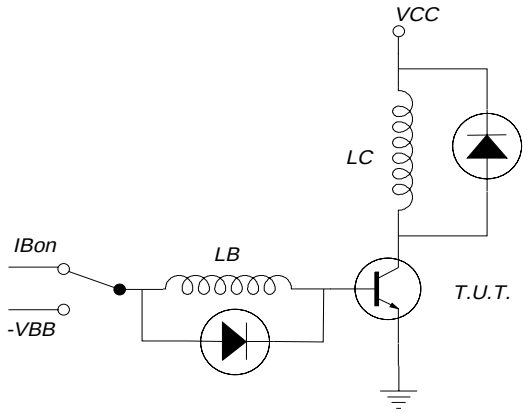


Fig.9. Test circuit inductive load. $V_{CC} = 300$ V; $-V_{BE} = 5$ V, $L_C = 200$ µH; $L_B = 1$ µH

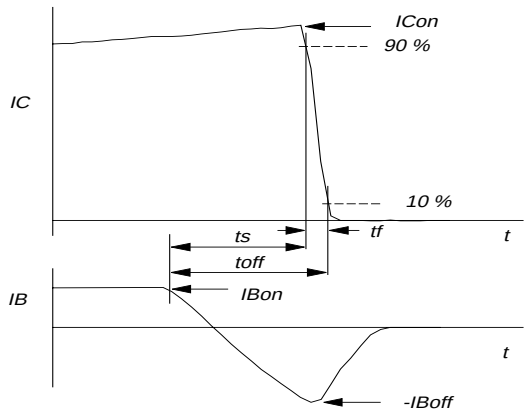


Fig.10. Switching times waveforms with inductive load.

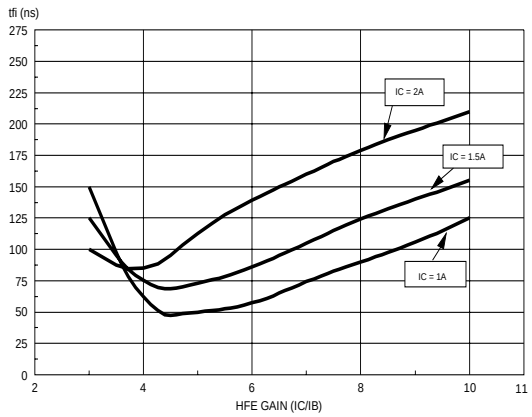


Fig.11. Inductive switching. $tfi = f(h_{FE})$

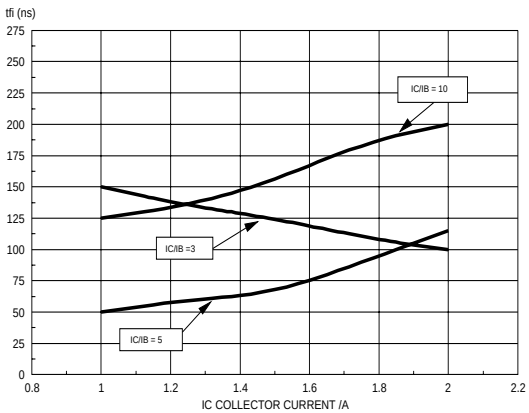


Fig.12. Inductive switching. $tfi = f(I_C)$

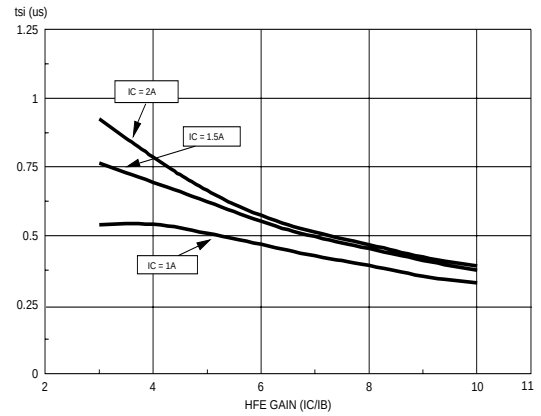


Fig.13. Inductive switching. tsi = f(h_{FE})

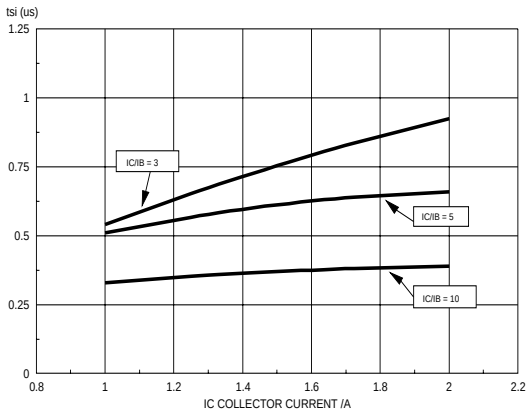


Fig.14. Inductive switching. tsi = f(I_C)

RESISTIVE SWITCHING

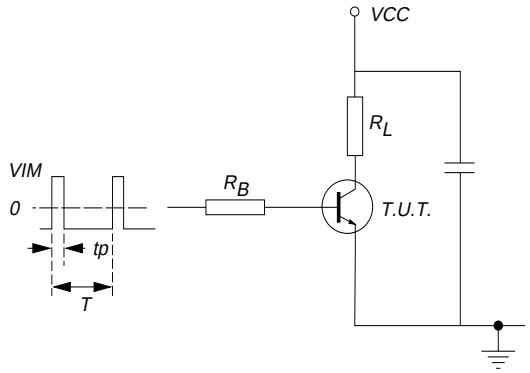


Fig.15. Test circuit resistive load. V_{IM} = -6 to +8 V V_{CC} = 250 V; t_p = 20 µs; δ = t_p / T = 0.01. R_B and R_L calculated from I_{Con} and I_{Bon} requirements.

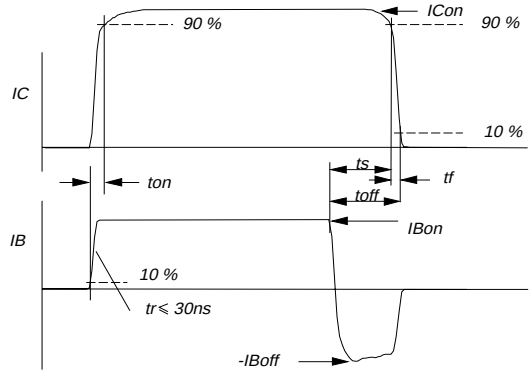


Fig.16. Switching times waveforms with resistive load.

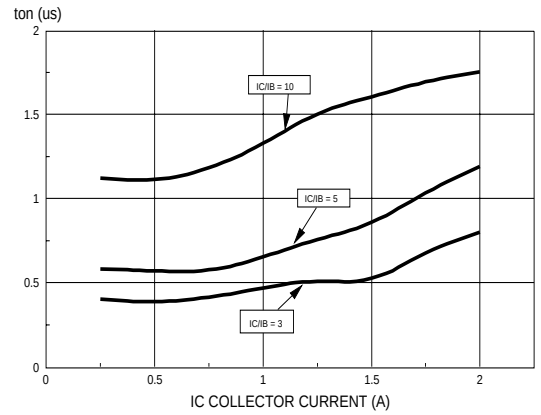


Fig.17. Resistive switching. ton = f(I_C)

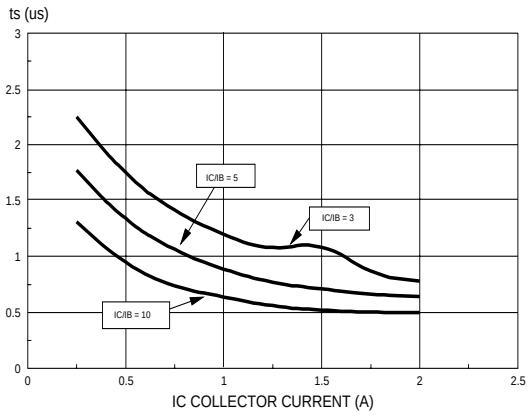


Fig.18. Resistive switching. ts = f(I_C)

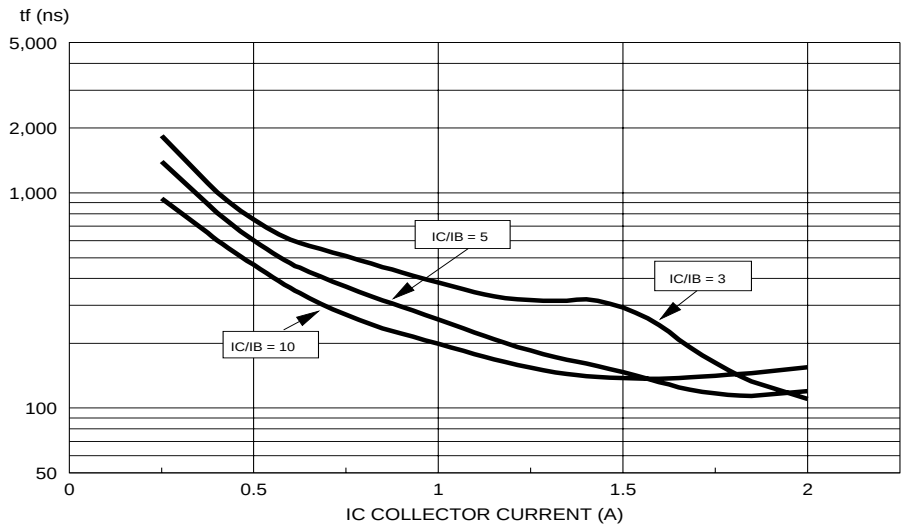


Fig.19. Resistive switching.
$tf = f(I_C)$

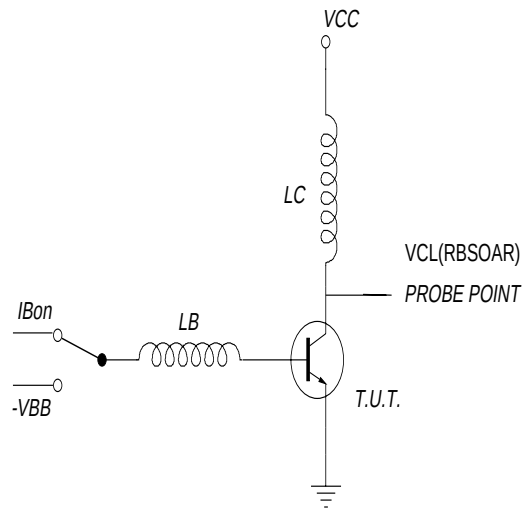


Fig.20. Test Circuit for the RBSOA test.
$V_{cl} \leq 700V$; $V_{cc} = 150V$; $L_B = 1\mu H$; $L_c = 200\mu H$

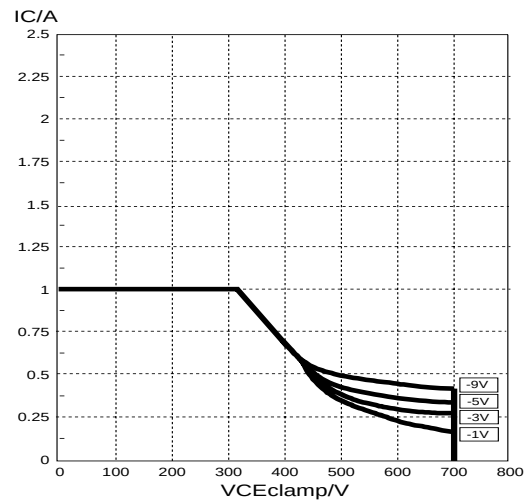


Fig.21. Reverse bias safe operating area $T_j \leq T_{jmax}$ for $-V_{BE}$ = 9V, 5V,3V & 1V

MOUNTING INSTRUCTIONS

Dimensions in mm.

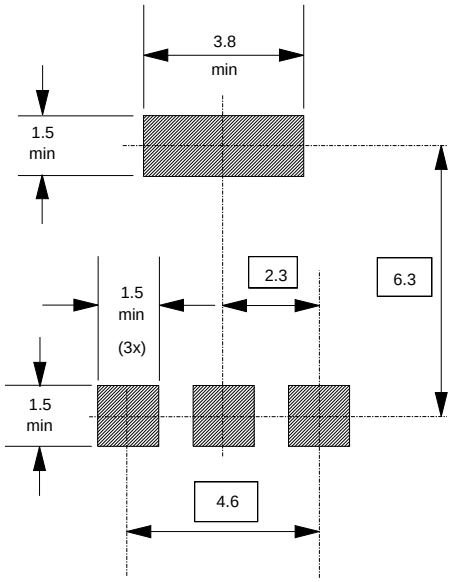


Fig.22. soldering pattern for surface mounting SOT223.

PRINTED CIRCUIT BOARD

Dimensions in mm.

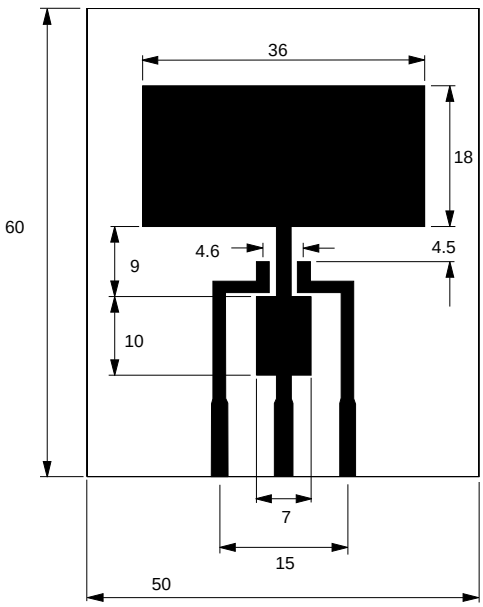
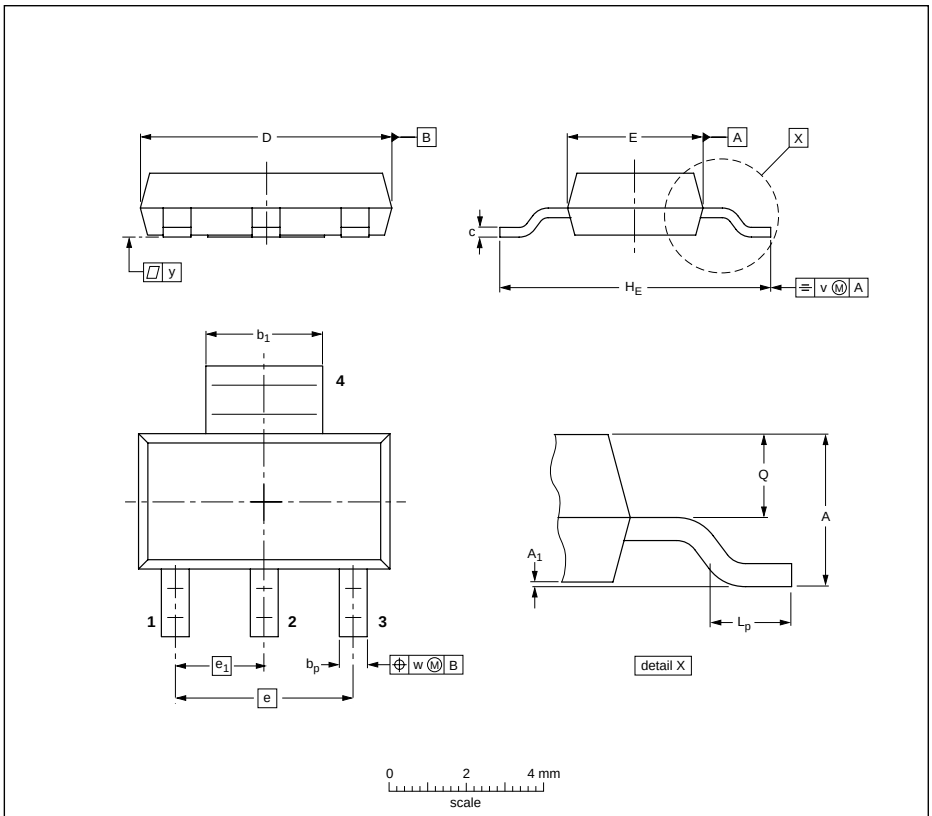


Fig.23. PCB for thermal resistance and power rating for SOT223.
PCB: FR4 epoxy glass (1.6 mm thick), copper laminate (35 μm thick).

MECHANICAL DATA

Plastic surface mounted package; collector pad for good heat transfer; 4 leads **SOT223**



DIMENSIONS (mm are the original dimensions)

UNIT	A	A_1	b_p	b_1	c	D	E	e	e_1	H_E	L_p	Q	v	w	y
mm	1.8 1.5	0.10 0.01	0.80 0.60	3.1 2.9	0.32 0.22	6.7 6.3	3.7 3.3	4.6	2.3	7.3 6.7	1.1 0.7	0.95 0.85	0.2	0.1	0.1

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT223						~~96-11-11~~ 97-02-28

Fig.24. SOT223 surface mounting package.

Notes

1. This product is supplied in anti-static packaging. The gate-source input must be protected against static discharge during transport or handling.
2. Refer to Discrete Semiconductor Packages, Data Handbook SC18.
3. Epoxy meets UL94 V0 at 1/8".

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values are given in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of this specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

LIFE SUPPORT APPLICATIONS

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